

Please make the following alterations to the User's Manual IM701450-01E.

■ Page i Add the FlexRay Signal Analyzer User's Manual

Manual Title	Manual No.	Description
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DL7440/DL7480 FlexRay Signal Analyzer User's Manual	IM 701450-52E	Describes the functions and procedures of the FlexRay bus signal analysis.

■ Page i Add a trademark description

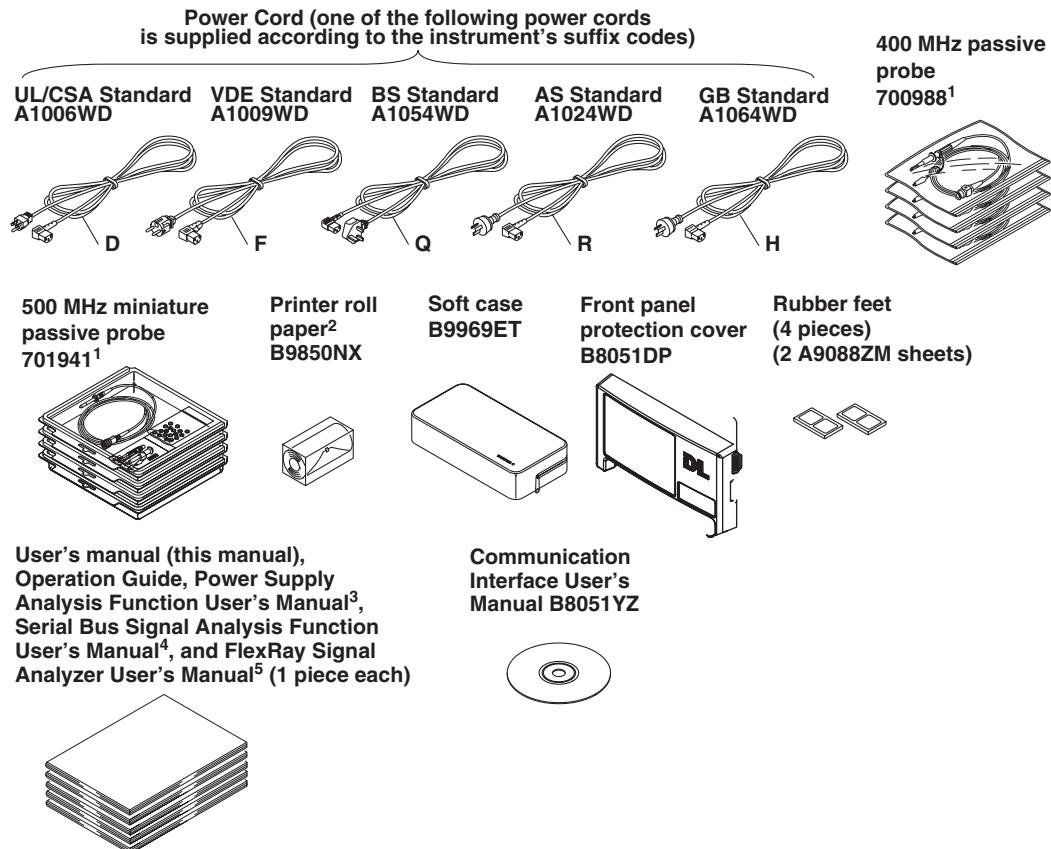
- FlexRay is either a registered trademark or trademark of Daimler Chrysler AG in the United States and/or other countries.

■ Page ii Add the suffix code of the FlexRay Signal Analyzer

Options
	/F9 FlexRay Signal Analyzer ⁸

8 When the /F9 option is specified, the marking on the DL7400 front panel changes to "FLEXRAY SIGNAL ANALYZER." In addition, the FLEXRAY key (SHIFT+MEASURE) is added.

■ Page iii Add the FlexRay Signal Analyzer User's Manual



1 On models with the /EX4 option, 701941 passive probes are provided in place of 700988 passive probes.

2 Provided on models with the /B5 option (built-in printer).

3 Provided on models with the /G4 option (power supply analysis function).

4 Provided on models with the /F5, /F7, or /F8 option (bus analysis function).

5 Provided on models with the /F9 option (FlexRay Signal Analyzer).

■ Page 9-24 Add the D/A conversion computation of the logic data to the user-defined computation
(The DA8 and DA12 operators are available on DL7400 firmware version 2.16 or later. The C-DA operator is available on version 2.40 or later.)

The logic data measured using the logic probe is handled as digital data of 8 bits or less or 12 bits or less, and an analog waveform is displayed through D/A conversion.

Add the following operators in the “Operator” section.

Operators and Examples		Computation
DA8	DA8(Ly,Z ₈)	Perform D/A conversion on the logic data of the specified number of bits (1 to 8) of L1 (Pod A) or L2 (Pod B).
DA12	DA12(Lx,Ly,Z ₁₀)	Perform D/A conversion on the logic data of the specified number of bits (9 to 12) of L1 (Pod A) or L2 (Pod B).
C-DA	C-DA(Lx,Ly,Z,W)	Perform D/A conversion on the logic data of the specified number of bits (1 to 12) of L1 (Pod A) or L2 (Pod B). The highest bit of Lx (A0 or B0) is detected as the clock bit.

* DA8 and DA12 are available on DL7400 firmware version 2.16 or later. C-DA is available on version 2.40 or later.

D/A Conversion of the Logic Data

- For Pod A and Pod B, A0 and B0 are assumed to be the highest bits and A7 and B7 are assumed to be the lowest bits.
- L1 and L2 indicate Pod A and Pod B, respectively.
- Performs D/A conversion on the logic data of the specified number of bits from the lowest bit.
- DA8 is set using the syntax DA8(Ly,Z₈).

Ly	L1 or L2
Z ₈ (number of bits)	1 to 8

- DA12 is set using the syntax DA12(Lx,Ly,Z₁₀).

Lx (higher bits)	L1 or L2, The highest 4 bits of Lx are always discarded.
Ly (lower bits)	L1 or L2
Z ₁₀ (number of bits)	9 to 12

- C-DA is set using the syntax C-DA(Lx,Ly,Z,W).

Lx (higher bits)	L1 or L2, The highest 4 bits of Lx are always discarded.
Ly (lower bits)	L1 or L2
Z (number of bits)	1 to 12

W (slope of the clock) 0 (rising edge), 1 (falling edge), 2 (both rising and falling edges)
The highest bit of Lx (A0 or B0) is detected as the clock bit. The logic data is sampled by synchronizing to this clock.

Example 1: Apply the clock (rising edge) to Pod A and perform D/A conversion on 8 bits of the Pod B data.

C-DA(L1,L2,8,0)

Example 2: Apply the clock (falling edge) to Pod A and perform D/A conversion on 7 bits of the Pod B data.

C-DA(L1,L1,7,1)

- The scaling is fixed to Auto. Manual scaling is not possible. The center and sensitive values according to the number of bits are as follows:

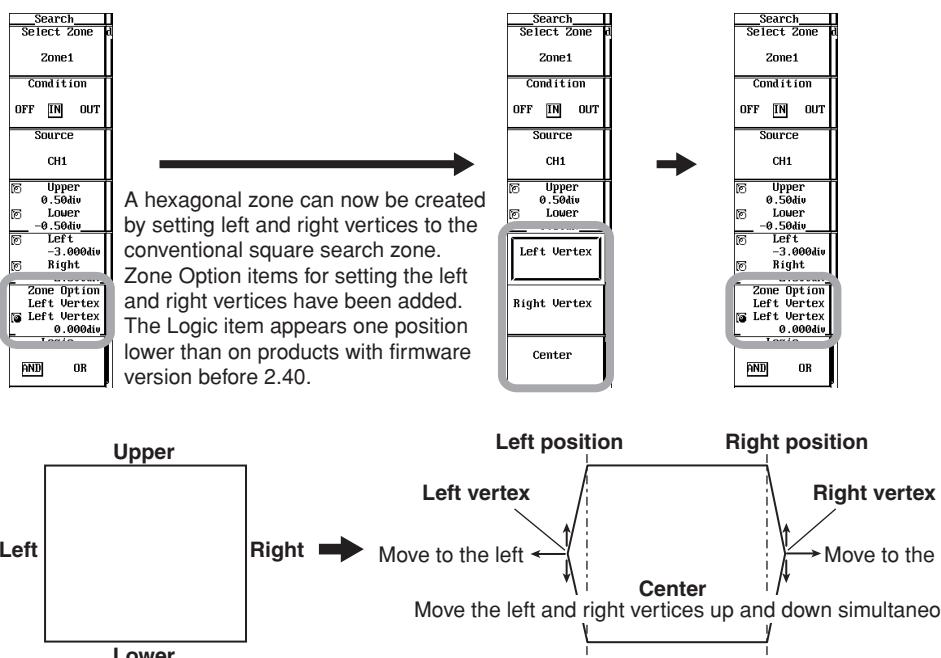
Bit Length	Center	Sensitivity	Significant Bits (Higher)	Significant Bits (Lower)
12 bits	2.0480E+03	7.6800E+02	X4 to X7	Y0 to Y7
11 bits	1.0240E+03	3.8400E+02	X5 to X7	Y0 to Y7
10 bits	5.1200E+02	1.9200E+02	X6 to X7	Y0 to Y7
9 bits	2.5600E+02	9.6000E+01	X7	Y0 to Y7
8 bits	1.28000E+02	4.8000E+01	–	Y0 to Y7
7 bits	6.4000E+01	2.4000E+01	–	Y1 to Y7
6 bits	3.2000E+01	1.2000E+01	–	Y2 to Y7
5 bits	1.6000E+01	6.0000E+00	–	Y3 to Y7
4 bits	8.0000E+00	3.0000E+00	–	Y4 to Y7
3 bits	4.0000E+00	1.5000E+00	–	Y5 to Y7
2 bits	2.0000E+00	7.5000E-01	–	Y6 to Y7
1 bit	1.0000E+00	3.7500E-01	–	Y7
				X, Y = A or B

■ Page 10-7 Add the function for creating hexagonal zones to the search zone of the history search (DL7400 firmware version 2.40 or later.)

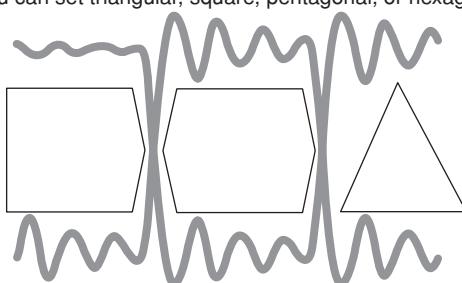
A function for setting the left and right vertices has been added to the conventional square search zone allowing you to create a hexagonal search zone. You can also set a triangular or a pentagonal zone.

Add the following steps between steps 13 and 14.

- 13-1. Press the **Zone Option** soft key to select Zone Option.
- 13-2. Press the **Zone Option** soft key again to display the Zone Option menu.
- 13-3. Press the **Left Vertex**, **Right Vertex**, or **Center** soft key to select the item you want to set.
 - Select Left Vertex to set the left vertex position.
 - Select Right Vertex to set the right vertex position.
 - Select Center to move the left and right vertices up and down.
- 13-4. Turn the **jog shuttle** to set the left and right vertex positions.



Example of a hexagonal zone
You can set triangular, square, pentagonal, or hexagonal zone.



■ Page 10-8 Add the following explanation.

Creating a Hexagonal Zone

You can set the left and right vertex positions of the search zone to set a hexagonal zone.

Left position of the left vertex

The selectable horizontal range is from the Left position to the left edge of the screen. The resolution is 10 divisions + the display record length. You cannot specify a position that is right of the Left position.

Right position of the right vertex

The selectable horizontal range is from the Right position to the right edge of the screen. The resolution is 10 divisions + the display record length. You cannot specify a position that is left of the Right position.

Vertical position of the left and right vertices

The selectable vertical range is between Upper and Lower positions. The resolution is 0.1%. Set the position by assuming the distance between the Upper and Lower positions to be 100%. The left and right vertices always move simultaneously in the vertical direction.